

**what is it?** microIOC Delay Generator is a **low-jitter delay generator** with **15 fully-programmable output channels**.

Every channel can have its delay and pulse width individually programmed with a time resolution of 1 ns. Signal delay can be set in the range of 1 ns – 4 s and signal width in the range of 1 ns – 4 s.

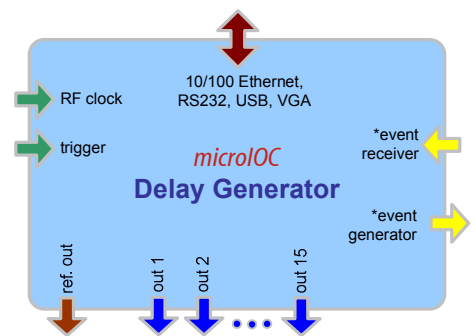
The value of the jitter is maintained at only 50 ps RMS, regardless of the settings.

Additional reference output is provided to determine system propagation delay. This delay is constant for all output channels and delay-time values.

Delay Generator output signals can be **synchronized with any of the following signals**:

- external RF-clock signal (50–500 MHz),
- AC line,
- external trigger signal,
- internal trigger signal.

\* Event receiver and generator functionality will be supported in future. Optical port with 8B/10B stream encoding will be used.



To provide compatibility with various subsystems, **different output voltage levels** are supported; PECL, TTL and optical interface are available. As microIOC Delay Generator is **fully digital design**, no time-consuming calibration of analogue delay lines required, which can be found at similar products.

Delay Generator configuration and status parameters (channel delay and pulse width, trigger/clock sources and channel busy alarm) are configured via microIOC standard interfaces.

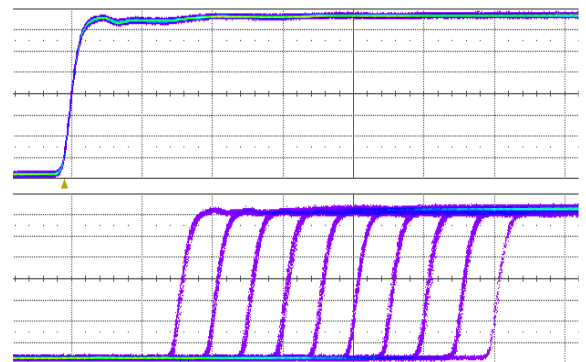


The following features are provided as standard: industrial-grade components; standard x86 architecture; dual Ethernet, 2xUSB, RS232, and VGA interfaces; complete SW support: Linux Debian or RTEMS, control system integration.

Please check microIOC baseline for the details of the microIOC family.

- benefits**
- 15 output channels
  - different output standards
  - completely digital design – no calibration
  - synchronization with various signals

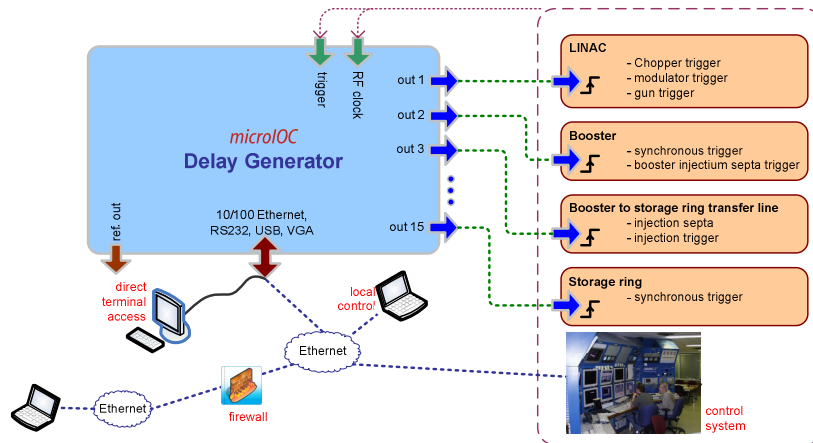
- key features**
- individually programmed output channels
  - time resolution: 1 ns
  - signal and pulse delay range: 1 ns – 4 s
  - constant jitter at only 50 ps RMS
  - microIOC family based product



Persistent snapshots of reference vs. output channel. Channel delay is incremented by 1ns steps. Oscilloscope time base is 2 ns/div.



- use case**
- designed for generation of accelerator's fast timing signals (i.e. bucket filling)
  - synchronization of beam-monitoring instrumentation, which has to be precisely synchronized with beam transition (e.g. beam position monitors, current transformers, profile monitors, etc.)



**technical specification**

microIOC Delay Generator	
<b>Trigger</b>	
<b>External trigger:</b> threshold impedance	programmable: -2.5 to 2.5 V in 100 mV steps or TTL configurable: 50 Ω / 1 MΩ
<b>Internal trigger:</b> configurability rate	0.01 Hz – 1 MHz
<b>AC line trigger:</b> division factor phase shift step phase shift range	1, 2,5 and 10 1 ms 0 – 20 ms
<b>External clock</b>	
frequency range	50 – 500 MHz
input level	PECL (AC coupled)
<b>Internal clock</b>	
frequency	500 MHz
jitter	10 ps max
<b>Output channels</b>	
<b>PECL differential:</b> number of channels connector type output impedance	7 + reference LEMO, HNG 50 Ω
<b>5V-TTL single-ended:</b> number of channels connector type output impedance	8 SMA 50 Ω
<b>Timing specifications</b>	
delay range	0 – 4 s
pulse width range	1 ns – 4 s
resolution	1 ns (future version: 125 ps)
jitter	50 ps RMS
propagation delay (input trigger → output)	~20 ns
<b>microIOC</b>	
CPU	x86 compatible AMD GEODE GX1, 300 MHz
interfaces	10/100 Ethernet, 2xUSB, RS232, VGA
SW	all drivers, Linux Debian, full control system integration (EPICS, ACS and Tango)
power supply	110/220 V (50/60 Hz), industrial grade, current protection

